



Astera Labs' Leo CXL Smart Memory Controllers on Microsoft Azure M-series Virtual Machines Overcome the Memory Wall

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SAN JOSE, Calif., Nov. 18, 2025 (GLOBE NEWSWIRE) -- Astera Labs, Inc. (Nasdaq: ALAB), a leader in semiconductor-based connectivity solutions for rack-scale AI infrastructure, today announced its Leo CXL Smart Memory Controllers enable customers to evaluate Compute Express Link® (CXL®) memory expansion capabilities for their specific workloads in the [Azure M-series virtual machines \(VMs\) preview](#).

Microsoft's Azure M-series VMs is the industry's first announced deployment of CXL-attached memory, addressing the growing demands of memory-intensive workloads, including in-memory databases. As organizations process increasingly large datasets, traditional server architectures face a fundamental bottleneck known as the "memory wall." CXL technology breaks through this barrier by enabling memory expansion beyond the limitations of CPU-attached DRAM, providing cloud providers and enterprises with the flexibility to scale memory capacity and performance.

Leo CXL Smart Memory Controllers support CXL 2.0 with up to 2TB of memory capacity per controller, enabling cloud providers to scale server memory capacity by more than 1.5x.¹ This addresses enterprise workloads such as in-memory databases and big data analytics, while also enabling AI inference applications, KV Cache storage for LLMs, machine learning workloads, and recommendation systems where large-scale memory capacity significantly reduces total cost of ownership.

"Our collaboration with Microsoft on CXL-attached memory for Azure M-Series virtual machines demonstrates our commitment to advancing memory connectivity solutions for cloud infrastructure," said Thad Omura, chief business officer for Astera Labs. "By enabling dramatically higher memory capacities, we unlock performance and scalability for a growing list of AI and in-memory databases—applications where memory is the ultimate constraint. Astera Labs aims to advance memory connectivity innovations that redefine what's possible in modern infrastructure."

"Addressing memory capacity constraints in cloud infrastructure requires deep collaboration to understand both the technical challenges and the operational demands of hyperscale deployment," said Rajesh Sankaran, distinguished engineer and vice president, Azure Hardware Systems & Architecture at Microsoft. "Astera Labs has been integral to advancing CXL capabilities for Azure, and their engagement—from early architectural discussions through platform integration—exemplifies the kind of collaboration essential for enabling new technologies."

For additional resources:

- **View detailed specifications for Leo CXL Smart Memory Controllers:** <https://www.asteralabs.com/products/leo-cxl-smart-memory-controllers/>
- **Learn more about the value Astera Labs' Leo CXL Smart Memory Controllers enable on Azure M-series VMs:** aka.ms/CXLTechMSeries
- **Explore how Astera Labs is advancing CXL with interoperable solutions:** <https://www.asteralabs.com/advancing-cxl-with-interoperable-solutions/>
- **Discover Astera Labs' flexible CXL product suite for low-latency memory expansion:** <https://www.asteralabs.com/astera-labs-flexible-cxl-product-suite-enables-low-latency-memory-expansion/>

About Astera Labs

Astera Labs (NASDAQ: ALAB) provides rack-scale AI infrastructure through purpose-built connectivity solutions grounded in open standards. By collaborating with hyperscalers and ecosystem partners, Astera Labs enables organizations to unlock the full potential of modern AI. Astera Labs' Intelligent Connectivity Platform integrates CXL®, Ethernet, PCIe®, and UALink™ semiconductor-based technologies with the company's COSMOS software suite to unify diverse components into cohesive, flexible systems that deliver end-to-end scale-up, and scale-out connectivity. Discover more at www.asteralabs.com.

Forward-Looking Statements

This communication contains certain forward-looking statements regarding Microsoft's deployment of Astera Labs' Leo CXL Smart Memory Controllers for Azure M-series VMs featuring CXL technology and the expected impact and benefits associated with this private preview. Such forward-looking statements are introduced using words such as "aims," "commitment," and "potential" and variations of such words and similar expressions. Such statements involve risks and uncertainties, many of which are beyond the control of Astera Labs and Microsoft, that could cause actual results to differ materially from those expressed or implied in the forward-looking statements, including, among others, the risk that the expected capabilities of the deployment may not be realized; delays, disruptions, challenges or increased costs in the solutions covered by the collaboration; the complexities and uncertainties in implementing solutions based on new technologies; litigation or disputes related to the collaboration or otherwise; macroeconomic conditions, including general semiconductor industry economic conditions; regulatory restrictions; international

conflict and other risks and uncertainties described in Astera Lab's Form 10-K, Form 10-Q and other filings with the SEC.

Forward-looking statements speak only as of the date they are made. Readers are cautioned not to put undue reliance on forward-looking statements, and no person assumes any obligation to update or revise any such forward-looking statements, whether as a result of new information, future events or otherwise, except to the extent that disclosure may be required by law.

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¹ Yuhong Zhong et al., "TPP: Transparent Page Placement for CXL-Enabled Tiered Memory," USENIX OSDI 2024, <https://www.usenix.org/system/files/osdi24-zhong-yuhong.pdf>



Source: ASTERA LABS, INC.