



## Astera Labs Extends Interoperability Leadership Driving Seamless PCIe 6.x Deployment

May 20, 2024

*New Cloud-Scale Interop Lab in Taiwan accelerates time-to-market for PCIe 6.x AI servers optimized with recently launched Aries 6 Smart DSP Retimers*

SANTA CLARA, Calif.--(BUSINESS WIRE)--May 20, 2024-- Astera Labs (Nasdaq: ALAB), a global leader in semiconductor-based connectivity solutions for AI and cloud infrastructure, today announced expanded PCIe® 6.x testing capabilities in its [Cloud-Scale Interop Lab](#) to enable seamless interoperability between [Aries 6 PCIe/CXL Smart DSP Retimers](#) and a broad range of PCIe 6.x hosts and endpoints. This paves the way for AI platform developers to design high-bandwidth, low-latency PCIe 6.x connectivity with confidence, reduce overall development time, and deploy at scale.

**Thad Omura, Chief Business Officer, Astera Labs, said,** "As AI systems continue to advance at a rapid pace, data center operators need to deploy increasingly complex systems on an accelerated timeline. Our intense focus on standards compliance and plug-and-play interoperability is foundational to why our widely deployed, field-tested Aries Retimer portfolio sets the gold standard for PCIe/CXL® connectivity. Expanding our Cloud-Scale Interop Lab test suite to support PCIe 6.x operation fast-tracks deployment for customers integrating Aries 6 – the industry's lowest power PCIe 6.x/CXL 3.x Retimer – with solutions from our ecosystem partners."

### Purpose-Built Connectivity Testing at Cloud-Scale

Higher bandwidth PCIe 6.x technology is required to maximize utilization of GPUs, CPUs, and AI accelerators to meet the performance demands of new AI workloads in hyperscale systems; however, this creates new connectivity issues with increases in speed, complexity, and scale. These challenges emphasize the need for extensive testing to ensure robust interoperability between the wide variety of PCIe 6.x components within an AI system deployed at cloud-scale.

For this reason, Aries 6 is put through a rigorous test suite to exercise the PCIe link with a series of loop tests over thousands of iterations and recreate end customers' real-world system configurations with leading root complexes and over 50 endpoints in complex PCIe topologies.

### Cloud-Scale Interop Lab Expands to Taiwan

Astera Labs has chosen Taiwan to launch its first Cloud-Scale Interop Lab outside of Silicon Valley given the region's rich collection of leading technology design and manufacturing companies. This new interop lab location will facilitate closer collaboration with key ODM customers to test Aries 6 in complex PCIe topologies with a broad variety of hosts and end points interconnected over varying channel insertion loss budgets in real systems.

**Brad Reger, VP & Principal Architect, Ingrasys Technology Inc. (a subsidiary of Foxconn Technology Group), said,** "Reliable interoperability is essential to accelerating the adoption of new interconnect protocols such as PCIe 6.x, which will make up the connectivity backbone of future AI and cloud infrastructure deployments. We look forward to continued collaboration with Astera Labs and leveraging its rigorously tested, field proven PCIe/CXL Retimer portfolio in our solutions."

**Vincent Lin, GM, Inventec EGB, said,** "We are proud to continue our deep relationship with Astera Labs as it adds PCIe 6.x testing and expands its interoperability lab into Taiwan. We look forward to tapping into its deep PCIe connectivity expertise to accelerate development of our critical data center solutions for the AI era."

**Mike Yang, Senior Vice President and General Manager, Quanta Computer Inc., said,** "Quanta values its close collaboration with Astera Labs to help our customers overcome emerging data center design challenges as AI and data-centric workload deployments continue to increase exponentially. Its robust Aries 6 Retimers tested in the new Taiwan Cloud-Scale Interop Lab will strengthen the roll-out of reliable PCIe 6.x connectivity in next generation AI and cloud infrastructure."

**William Lin, President of Enterprise and Networking Business Group, Wistron, said,** "With growing demand for our AI and HPC servers, we turn to Astera Labs' gold standard PCIe/CXL Retimer portfolio to deliver robust reach extension for our solutions destined to customer deployments. We have leveraged multiple generations of Aries Retimers in our products, and we are excited to continue our partnership as it paves the way for highly interoperable PCIe 6.x/CXL 3.x connectivity leveraging Aries 6 that is tested in the new Taiwan Cloud-Scale Interop Lab."

**Steven Lu, Executive Vice President, Wiwynn, said,** "Wiwynn is excited to see Astera Labs extend its cloud-scale testing capabilities with the launch of the new Taiwan Interop Lab. It will enable closer collaboration and accelerate the deployment of seamless plug-and-play PCIe 6.x connectivity for AI. We look forward to strengthening our partnership to ensure reliable interoperability and meet hyperscalers' needs for our future PCIe 6.x systems."

### Resources:

- [Aries Cloud-Scale Interop Lab \[Webpage\]](#)
- [Aries PCIe/CXL Smart DSP Retimers \[Webpage\]](#)
- [Why We Test \[Video\]](#)
- [How We Test \[Video\]](#)

### About Astera Labs

Astera Labs is a global leader in purpose-built connectivity solutions that unlock the full potential of AI and cloud infrastructure. Our Intelligent Connectivity Platform integrates PCIe®, CXL®, and Ethernet semiconductor-based solutions and the COSMOS software suite of system management and optimization tools to deliver a software-defined architecture that is both scalable and customizable. Inspired by trusted relationships with hyperscalers and the data center ecosystem, we are an innovation leader delivering products that are flexible and interoperable. Discover how we are

transforming modern data-driven applications at [www.asteralabs.com](http://www.asteralabs.com).

© Astera Labs, Inc. Astera Labs, and its stylized logo, are trademarks of Astera Labs, Inc. or its affiliates. Other names and brands may be claimed as the property of others.

View source version on [businesswire.com](http://businesswire.com): <https://www.businesswire.com/news/home/20240519095633/en/>

Joe Balich

[Joe.balich@asteralabs.com](mailto:Joe.balich@asteralabs.com)

Source: Astera Labs