Astera Labs Introduces Industry's First CXL™ 2.0 Memory Accelerator SoC Platform

November 15, 2021

Leo CXL ™Memory Accelerator Technology Ushers in a New Generation of Tiered Memory for Servers, Solves Memory Capacity and Bandwidth Bottlenecks in Data Centers and the Cloud

SANTA CLARA, Calif.--(BUSINESS WIRE)--Astera Labs, a pioneer in connectivity solutions for intelligent systems, today announced its new Leo Memory Accelerator Platform for Compute Express Link™ (CXL™) 1.1/2.0 interconnects to enable robust disaggregated memory pooling and expansion for processors, workload accelerators, and smart I/O devices. Leo overcomes processor memory bandwidth bottlenecks and capacity limitations while offering built-in fleet management and deep diagnostic capabilities critical for large scale enterprise and cloud server deployments.

"CXL is a true game changer for hyperscale data centers, enabling memory expansion and pooling capabilities to support a new era of data-centric and composable compute infrastructure," said Jitendra Mohan, CEO, Astera labs. "We have developed the Leo SoC platform in lockstep with leading processor vendors, system OEMs, and strategic cloud customers to unleash the next generation of memory interconnect solutions."

CXL is a foundational standard and is proving to be a critical enabler to realize the vision of AI in the cloud. Astera Labs is a proud contributor to this exciting technology and is working with key industry leaders developing the CXL technology to accelerate the development and deployment of a robust ecosystem.

"The introduction of CXL provides a critical capability to create a unified, coherent memory space between CPUs and accelerators, and this innovation will revolutionize how data center server architectures will be built for years to come," said Jim Pappas, Director of Technology Initiatives at Intel. "Astera Labs' Leo CXL Memory Accelerator Platform is an important enabler for the Intel ecosystem to implement a shared memory space between hosts and attached-devices."

As the industry's first CXL SoC solution to implement the CXL.memory (CXL.mem) protocol, the Leo CXL Memory Accelerator Platform allows a CPU to access and manage CXL-attached DRAM and persistent memory, enabling the efficient utilization of centralized memory resources at scale without impacting performance.

"AMD recognizes the tremendous value that CXL brings to heterogeneous computing to meet the industry's need for increased compute capacity and faster data processing through resource disaggregation," said Michael Hall, director of customer compatibility, AMD. "Solutions like Astera Labs' Leo Memory Accelerator Platform are critical to enable tighter coupling between AMD processors, accelerators and memory expansion."

The Leo Platform of ICs and hardware increases overall memory bandwidth by 32 GT/s per lane and capacity up to 2TB, maintains ultra-low latency, and provides server class RAS features for robust and reliable cloud scale operation.

"To continue to enable the rapid growth of heterogeneous computing, we need to remove barriers such as the cost of scaling memory and highspeed interconnects across enterprise, hyperscaler, storage and accelerator applications," said John DaCosta, senior director, strategic segments, Arm. "Arm sees CXL as a significant driver in this space, and Astera Labs' new platform will help to address these needs in cloud and edge computing data centers using Arm®-based technology."

Astera Labs continues to bridge the next wave of hyperscale data center innovation through its unmatched CXL connectivity expertise and focus on seamless ecosystem interoperability.

"Astera Labs has been a valuable member to the CXL Consortium contributing its expertise in enabling connectivity for heterogeneous compute architectures," said Barry McAuliffe, CXL Consortium President. "We are pleased to see Astera Labs launch its first CXL memory expansion and pooling solution to support the rapidly expanding CXL ecosystem."

Building on the success of its Aries CXL Smart Retimers, the Leo CXL Memory Accelerator Platform extends Astera Labs' family of solutions that unlock the CXL interconnect's true potential. The company's breakthrough solution portfolio now encompasses several complimentary product families that enable connectivity for modern data-centric systems based on complex heterogeneous compute architectures and composable disaggregation topologies.

Visit www.AsteraLabs.com or contact info@AsteraLabs.com for more information on its CXL connectivity solutions.

Resources:

- Unlock the Full Potential of CXL™ with Purpose-Built Connectivity Solutions from Astera Labs (VIDEO)
- Leo CXL™ Memory Accelerator Platform Introduction and CXL Interop Demo (VIDEO)
- Connectivity Is Key to Harnessing the Data Reshaping Our World (PAPER)

About Astera Labs

Astera Labs Inc., a fabless semiconductor company headquartered in the heart of California's Silicon Valley, is a leader in purpose-built connectivity solutions for data-centric systems throughout the data center. The company's product portfolio includes system-aware semiconductor integrated circuits, boards, and services to enable robust CXL, PCIe, and Ethernet connectivity. For more information about Astera Labs including open positions, visit www.AsteraLabs.com.

Contacts

Joe Balich
astera@nereus-worldwide.com