



Astera Labs Enters Pre-Production Phase of Leo Memory Connectivity Platform for CXL-Attached Memory Expansion and Pooling

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SANTA CLARA, Calif.—[Astera Labs](#), a pioneer in purpose-built connectivity solutions for intelligent systems, today announced its Leo Memory Connectivity Platform supporting Compute Express Link™ (CXL™) 1.1 and 2.0 has begun pre-production sampling for customers and strategic partners to enable secure, reliable and high-performance memory expansion and pooling for cloud servers. This milestone follows the successful end-to-end interoperability testing of the Leo Smart Memory Controllers with industry-leading CPU/GPU platforms and DRAM memory modules over a variety of real-world workloads.

“Our Leo Memory Connectivity Platform for CXL 1.1 and 2.0 is purpose-built to overcome processor memory bandwidth bottlenecks and capacity limitations in accelerated and intelligent infrastructure,” said Jitendra Mohan, CEO, Astera Labs. “Successful delivery of Leo Smart Memory Controllers, Leo-based hardware board solutions and comprehensive software tools to our partners and customers represents a significant industry-first milestone by paving the way for a seamless, at-scale deployment of memory pooling and expansion in the Cloud.”

CXL is proving to be a critical enabler to realize the vision of Artificial Intelligence (AI) and Machine Learning (ML) in the cloud. Leo Smart Memory Controllers implement the CXL.memory (CXL.mem) protocol to allow a CPU to access and manage CXL-attached memory in support of general-purpose compute, AI training and inference, machine learning, in-memory databases, memory tiering, multi-tenant use-cases, and other application-specific workloads.

“Applications like Artificial Intelligence, Machine Learning and in-memory database managers have an insatiable appetite for memory, but current CPU memory buses limit DRAM capacity to eight DIMMs per CPU,” observed Nathan Brookwood, research fellow at Insight 64. “CXL promises to free systems from the constraints of motherboard memory buses, but requires that CPUs and DRAM controllers be reengineered to support the new standard. Forthcoming processors from AMD and Intel address the CPU side of the link. Astera’s Leo Smart Memory Controllers are available now and address the other end of the CXL link. In just a few months, cloud providers and OEMs will be rolling out a new generation of servers with DRAM capacities customers could only dream about until now.”

Leo Smart Memory Controllers offer comprehensive features that hyperscale data centers require for cloud-scale deployment of compute-intensive workloads, such as AI and ML. Leo provides server-grade customizable Reliability, Availability and Serviceability (RAS) capabilities to enable data center operators to tailor their solutions so factors such as memory errors, material degradation, environmental impacts, or manufacturing defects do not impact application performance, uptime, and user experience. Extensive telemetry features and software APIs for fleet management make it easy to manage, debug and deploy at scale on cloud-based platforms. Unlike other memory expansion solutions, Leo supports end-to-end datapath security and unleashes the highest capacity and bandwidth by supporting up to 2TB of memory per Leo Controller and up to 5600MT/s per memory channel, the minimum speed required to fully utilize the bandwidth of the CXL 1.1 and 2.0 interface.

“CXL is designed to be an open standard interface to support composable memory infrastructure that can expand and share memory resources to bring greater efficiency to modern data centers,” said Raghu Nambiar, corporate vice president, Data Center Ecosystems and Solutions, AMD. “We’re excited to work closely with Astera Labs on the development of their Leo Memory Connectivity Platform to deliver interoperability and robust validation with AMD processors and accelerators.”

Leo Smart Memory Controllers feature a flexible memory architecture that ensures support for not only JEDEC standard DDR interface, but also for other memory vendor-specific interfaces providing unique flexibility to support different memory types, and achieving lower total cost of ownership (TCO). Leo Smart Memory Controllers are also the industry’s first solution to address memory pooling and sharing to allow data center operators to further reduce TCO by increasing memory utilization and availability.

“CXL provides a platform for a wealth of memory connectivity options and innovations in next-generation server architectures, which is essential for the industry to realize the tremendous potential of data-centric applications,” said Zane Ball, Corporate Vice President, and General Manager, Data Platforms Engineering and Architecture Group, Intel. “Our continued collaboration with the CXL ecosystem providers, such as Astera Labs through their Leo Memory Connectivity Platform, will help enable customers to develop reliable, interoperable CXL memory expansion and pooling solutions.”

Leo Smart Memory Controllers have been developed in close partnership with the industry’s leading processor vendors, memory vendors, strategic cloud customers, system OEMs, and the CXL Consortium to ensure they meet their specific requirements and seamlessly interoperate across the ecosystem.

“Astera Labs continues to be a valuable contributor to the CXL Consortium with its connectivity expertise and commitment to vendor-neutral interoperability,” said Siamak Tavallaei, president, CXL Consortium. “We’re excited to see Astera Labs deliver a solution to help enable a rapidly growing marketplace of CXL memory expansion and pooling products.”

Astera Labs Leo Memory Connectivity Platform for CXL-attached memory offers the following product solutions:

- Leo E-Series Smart Memory Controllers supporting memory expansion
- Leo P-Series Smart Memory Controllers supporting memory expansion, pooling, and sharing
- Aurora A-Series Smart Memory Hardware Solutions – PCIe CEM Add-in Card for plug-and-play deployment of Leo Smart Memory Controllers

Development and Evaluation:

Astera Labs has released extensive product documentation, application notes, firmware, software, management utilities and development kits to enable partners and customers to seamlessly evaluate, develop and deploy Leo Smart Memory Controllers and Aurora A-Series Smart Memory Hardware Solutions.

Astera Labs will demonstrate the Leo Memory Connectivity Platform at VMware Explore 2022 US this week as part of the [“How Your Future Server Purchase Should Be Ready for Tiered Memory”](#) session alongside Lenovo and VMware.

Resources:

- [\[Video Link\]](#) Leo Memory Connectivity Platform: First Look Demo
- [\[Video Link\]](#) Unlock the full potential of CXL with the Leo Memory Connectivity Platform
- [\[Product Brief Link\]](#) Leo Memory Connectivity Platform Product Brief
- [\[Product Page Link\]](#) Leo Memory Connectivity Platform Product Page
- [\[Blog\]](#) Unlocking Cloud Server Performance with CXL

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About Astera Labs

Astera Labs is a global leader in purpose-built connectivity solutions that unlock the full potential of cloud and AI infrastructure. Our Intelligent Connectivity Platform integrates PCIe, CXL and Ethernet semiconductor-based solutions based on a software-defined architecture that is both scalable and customizable. Inspired by trusted partnerships with hyperscalers and the data center ecosystem, we are an innovation leader of products that are flexible, interoperable, and reliable. Discover how we are transforming modern data-driven applications at www.asteralabs.com.

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CONTACT: Joe Balich
joe.balich@asteralabs.com