



Astera Labs Launches Cloud-Scale Interop Lab to Enable Seamless Deployment of CXL Solutions at Scale

January 31, 2023

Partnering with industry-leading CPU and memory vendors, Astera Labs extends leadership in interoperability testing so system integrators can deploy CXL-attached memory with confidence

SANTA CLARA, CA, U.S. – January 31, 2023 – [Astera Labs](#), the industry-leader for purpose-built connectivity solutions, today announced the expansion of its Cloud-Scale Interop Lab to provide robust interoperability testing between its [Leo Memory Connectivity Platform](#) and a growing ecosystem of leading CXL-based CPUs, memory modules, and operating systems.

"Compute Express Link™ (CXL™) is proving to be a critical memory interconnect technology in data-centric systems; however, multiple use cases and a fast-growing ecosystem is proving to be a significant challenge for seamless deployment of CXL solutions at scale," said Casey Morrison, CPO, Astera Labs. "Building on the success of our Cloud-Scale Interop Lab for Aries PCIe® Smart Retimers and learnings from real CXL silicon solutions working on customer platforms, we are excited to partner with industry leaders to implement end-to-end CXL tests and tools to minimize interoperation risk, reduce system development time and costs, and accelerate time-to-market."

The Cloud-Scale Interop Lab utilizes a comprehensive suite of memory stress tests, CXL protocol checks, and electrical robustness measurements to validate performance and interoperability between CPUs, Leo Smart Memory Controllers, and a variety of memory modules in real-world use cases. The testing covers four key areas spanning from the physical layer to the application layer, including PCIe electrical, memory, CXL compliance and system-level testing over thousands of iterations. Customers can request the reports at www.AsteraLabs.com/GetReports.

Cloud-Scale Interop Lab Key Partnerships

Astera Labs is collaborating on interop testing with industry leaders delivering CPUs and memory modules for the growing CXL market.

Jim Pappas, Chairman, CXL Consortium, said: "The CXL Consortium hosts events that test member company products for compliance to our specifications. With its Cloud-Scale Interop Lab, Astera Labs extends that testing with rigorous interoperability tests from the physical level to the system level with a broad range of hosts, memory and operating systems. As a CXL Consortium contributor member, Astera Labs' vendor-neutral approach will help accelerate the delivery of CXL memory solutions to market."

Mahesh Wagh, Senior Fellow, Server Systems Architect, AMD, said: "Both standards compliance and plug-and-play capabilities are an important step toward growing the CXL ecosystem. 4th Gen AMD EPYC™ processors are compatible with CXL 1.1 standards and help to create composable architectures that provide the infrastructure flexibility, security and performance requirements our customers demand. We applaud Astera Labs for its commitment to interoperability testing and look forward to our continued collaboration toward delivering truly heterogeneous computing."

Dr. Debendra Das Sharma, Senior Fellow, Intel Corporation, said: "Intel is committed to accelerating the CXL ecosystem, and we are looking forward to continuing our collaboration with Astera Labs and participating in its Cloud-Scale Interop Lab so our customers can more easily deploy reliable and interoperable CXL solutions."

Raj Hazra, Senior Vice President and General Manager of Micron's Compute and Networking Business Unit, said: "Micron is delivering memory innovations for the data center that leverage CXL, and we are collaborating with Astera Labs to test our DDR memory solutions in its Cloud-Scale Interop Lab. Together, we are alleviating the memory bandwidth bottleneck and providing interoperable solutions that result in greater flexibility for data center and cloud infrastructure customers."

Hyungsoo Kim, VP and Head of DRAM Application Engineering Group at SK hynix, said: "Our broad portfolio of high-performance and high-density DDR5 DRAM unlocks the full potential of CXL-attached memory expansion and pooling for cloud servers. With contributions from both Headquarters and US Engineering Center, SK hynix is excited to partner with Astera Labs to validate our memory in its Cloud-Scale Interop Lab, to enable our customers to gain assurance that our solution will interoperate seamlessly with Astera Labs' CXL Controller and customers' CPU of choice."

Resources:

- Website: [Cloud-Scale Interop Lab](#)
- Infographic: [Why We Test](#)
- Video: [How We Test](#)
- Video: [Interop Bulletin #1](#)

About Astera Labs

Astera Labs is a global leader in purpose-built connectivity solutions that unlock the full potential of cloud and AI infrastructure. Our Intelligent Connectivity Platform integrates PCIe, CXL and Ethernet semiconductor-based solutions based on a software-defined architecture that is both scalable and customizable. Inspired by trusted partnerships with hyperscalers and the data center ecosystem, we are an innovation leader of products that are flexible, interoperable, and reliable. Discover how we are transforming modern data-driven applications at www.asteralabs.com.

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