



Astera Labs First to Break Through the Memory Wall with Industry's Highest Performance CXL Memory Controllers

September 19, 2023

Increase memory bandwidth by 50% and reduce latency by 25% with Intel's server platforms

SANTA CLARA, CA, U.S. – September 19, 2023 – [Astera Labs](#), the global leader in semiconductor-based connectivity solutions for AI infrastructure, today announced that its Leo Memory Connectivity Platform enables data center servers with unprecedented performance for memory intensive workloads. Leo is the industry's first Compute Express Link™ (CXL™) memory controller that increases total server memory bandwidth by 50% while also decreasing latency by 25% when integrated with the forthcoming 5th Gen Intel® Xeon® Scalable Processor. Through new hardware-based interleaving of CXL-attached and CPU native memory, Astera Labs and Intel eliminate any application-level software changes to augment server memory resources via CXL. Existing applications can effortlessly "plug-and-play" to take advantage of the highest possible memory bandwidth and capacity in the system.

"The growth of computing cores and performance has historically outpaced memory throughput advancements, resulting in degraded server performance efficiency over time," said Sanjay Gajendra, COO of Astera Labs. "This performance scaling challenge has led to the infamous 'memory wall,' and thanks to our collaboration with Intel, our Leo Memory Connectivity Platform breaks through this barrier by delivering on the promise of PCIe 5.0 and CXL memory."

Data center infrastructure scaling limitations due to the memory wall are none more evident than in AI servers where memory bandwidth and capacity bottlenecks result in inefficient processor utilization. The CXL innovations delivered by Astera Labs and Intel directly address these bottlenecks and lay the foundation for cloud, hybrid-cloud and enterprise data centers to maximize accelerated computing performance.

Extending leadership of PCIe® 5.0 and CXL 2.0 solutions

Astera Labs has a history of delivering industry-first solutions that are critical to advancing the PCIe and CXL ecosystems. In addition to memory performance advancements with Leo, Astera Labs is also driving interoperability leadership with its Aries PCIe 5.0 / CXL 2.0 Smart Retimers on state-of-the-art Intel server platforms. As the most widely deployed and proven PCIe/CXL retimer family in the industry, Aries features a low-latency CXL mode that complements Leo to form the most robust CXL memory connectivity solution.

"We applaud Astera Labs for their contributions to the CXL ecosystem and are delighted to extend our ongoing collaboration. We believe Memory Connectivity Platforms containing innovations from companies like Astera Labs will help deliver enhanced performance on next generation Intel Xeon processors, and accelerate a myriad of memory intensive workloads," said Zane Ball, Corporate Vice President and General Manager, Data Center Platform Engineering and Architecture Group, Intel.

Visit Astera Labs at Intel Innovation!

Astera Labs will showcase Leo and Aries together with Intel's latest Xeon® Scalable processors at Booth #210, September 19-20 at the San Jose Convention Center. Talk to Astera Labs' experts to learn more about industry benchmarks and how to optimize PCIe/CXL memory solutions in data center architectures to deliver optimized performance for applications ranging from AI, real time analytics, genomics and modeling.

Resources:

- Webpage: [Leo Memory Connectivity Platform](#)
- Webpage: [Aries Smart Retimers](#)
- Webpage: [Cloud-Scale Interop Lab](#)

© Astera Labs, Inc. Astera Labs, its stylized logo, and Leo Memory Connectivity Platform are trademarks of Astera Labs, Inc. or its affiliates. Other names and brands may be claimed as the property of others.

Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries.

About Astera Labs

Astera Labs is a global leader in purpose-built connectivity solutions that unlock the full potential of cloud and AI infrastructure. Our Intelligent Connectivity Platform integrates PCIe, CXL and Ethernet semiconductor-based solutions based on a software-defined architecture that is both scalable and customizable. Inspired by trusted partnerships with hyperscalers and the data center ecosystem, we are an innovation leader of products that are flexible, interoperable, and reliable. Discover how we are transforming modern data-driven applications at www.asteralabs.com.

CONTACT: Joe Balich
joe.balich@asteralabs.com